The Correlated Level Shifting as a Gain Enhancement Technique for Comparator Based Integrators

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Abstract - This paper shows that correlated level shifting (CLS) technique can be successfully used in the comparator based integrators with the same benefits as in the conventional integrators. With help of CLS technique the signal dependent variation reduces by making current source work in the more voltage headroom region thus an output impedance of the current source is increasing. The latter leads to high gain of the system and more linear voltage ramp by the current source. This technique is especially used in the deep sub-micron technologies with the supply voltage below 1V, where headroom of a current source is low. Proposed comparator-based integrator is using comparator with about 27dB of gain which translates into 54dB of effective gain. Integrator was used to design the MASH sigma delta modulator which achieved SQNR of 86.0 dB at an OSR of 64.

Keywords - comparator-based integrators, sigma-delta modulator, correlated level shifting

I. INTRODUCTION

Switched-capacitor circuit techniques are widely used in many applications including filtering and analog-to-digital conversion. Performance of the last relies on achieving good capacitor matching and high opamp DC gain, both limiting the achievable accuracy of such circuits. Due to low gain of op-amps inverting inputs of its do not getting close each other (e.g. condition of the virtual zero is not satisfied) causing errors in the charge transfer phase. This error can be crucial depending on its applications. For example in the filters using low gain op-amps causes errors in both amplitude and phase response. In application like ADCs and DACs finite op-amp gain limits resolution and requirements in such converters is an order of magnitude higher than in the filters.

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Producing well-matched capacitor is easy in the advanced CMOS technologies. However, because of the decreasing supply voltage, designing high-gain and high-bandwidth operational amplifiers with good output swing is becoming more difficult, as cascoding of devices limits output signal swing. Many techniques have been proposed to overcome the low gain opamp issue. One of those techniques is to use comparator-based switched capacitor circuits. The comparator-based switched capacitor circuits (CBSC) suffer from signal dependent variation of the current source and overshoot due to the comparator delays as shown in [1].

II. CONVENTIONAL INTEGRATORS WITH USE OF CLS TECHNIQUE

Let's see how the correlated level shifting technique is working on the conventional integrators. In the CLS technique, the sampling phase (Fig. 1(a)), φ_1, is the same as for the switched-capacitor integrator of the conventional one (without CLS). The difference between the CLS and non-CLS circuit occurs in the charge-transfer phase, φ_2, which is subdivided into coarse and fine charge-transfers for the CLS case. During the coarse charge-transfer (Fig. 1(b)), the opamp (a.k.a Operational Amplifier) settles as for the non-CLS switched-capacitor integrator. However, at the end of this settling, the output voltage, V_{out}, is sampled onto capacitor C_{CLS} as a coarse estimate of the final value of V_{out}. During the fine charge-transfer (Fig. 1(c)), the voltage sampled onto C_{CLS} is used as an offset between the output of the opamp and node V_{out}. Due to this correlated level shifting, the voltage at the output of the opamp depends only on the difference between the coarse estimation of V_{out} and the final value of V_{out}. The transfer function of the integrator in the Z domain given an op-amp DC gain of A, can be written as [7]

$$\frac{V_{out}}{V_{in}} = \left(\frac{C_{in}}{C_{fb}}\right)\left[\frac{(1-\delta)z^{-1}}{1-(1-\alpha)z^{-1}}\right] \quad (1)$$

where

$$\delta = \frac{1}{1 + A\beta(1 + A)} ;$$

$$\alpha = \frac{1 - \beta}{1 + A\beta(1 + A)} \; and \; \beta = \frac{C_{fb}}{C_{in} + C_{fb}}$$

This decreased dependence on V_{out} reduces the effects of limited opamp gain, and potentially increases the swing of V_{out} beyond the range possible if V_{out} was directly driven by the opamp. The swing at the output of the op-amp will depend on the ratio of the level shifting capacitance to the total capacitance at the output. The larger the level shifting capacitor, the lower the swing but the higher the op-amp power consumption. Thus, there is a trade-off between the op-amp swing requirement and power consumption when choosing C_{CLS} .

III. CORRELATED LEVEL-SHIFTING IN CBSC CIRCUITS

We are proposing to use correlated level-shifting technique in comparator based switched capacitor circuits as well, expecting to have the same improvements in the output resistance of the current source and the effective gain of integrator.

In this technique, I_{fine} is not directly connected to node V_{out} but instead is capacitively coupled via capacitor C_{CLS}. During the coarse charge-transfer phase, an extra switch is closed, setting the voltage across C_{CLS} equal to the coarse estimation of V_{out}. This switch is then opened for the fine charge-transfer phase to be completed.

During the fine charge-transfer, when I_{fine} is used to set V_{out}, the voltage seen by I_{fine} is level-shifted through C_{CLS} by a voltage equal to the coarse estimation of V_{out}. Thus, the voltage across current source I_{fine} at the start of the fine charge-transfer is $V_{DD} - V_{SS}$. The change in voltage across I_{fine} during the fine charge-transfer phase is only a function of the coarse overshoot, removing the dependence of current I_{fine} on the full value of V_{out}. Because the coarse overshoot is relatively constant, I_{fine} becomes much more constant. With this correlated level-shifting, the current I_{fine} at the end of the fine charge-transfer becomes.

$$I_{fine} = I_{fine0} - \left(\frac{C_{FB}C_{CLS} + C_{IN}C_{CLS} + C_{FB}C_{IN}}{C_{FB}C_{CLS} + C_{IN}C_{CLS}}\right) \times \left(\frac{V_{overshoot,coarse}}{r_o}\right)$$

$$= I_{fine0} - \left(\frac{C_{FB}C_{CLS} + C_{IN}C_{CLS} + C_{FB}C_{IN}}{C_{FB}C_{CLS} + C_{IN}C_{CLS}}\right) \times \left(\frac{\frac{dV_{out}}{dt_{coarse}} t_{delay,coarse}}{r_o}\right) \quad (2)$$

where $\frac{dV_{out}}{dt_{coarse}}$ is the ramp rate of V_{out} and $t_{delay,coarse}$ is the delay of the comparator during the coarse charge-transfer. If $t_{delay,coarse}$ is a constant, then the only dependence of I_{fine} on V_{out} now comes from $\frac{dV_{out}}{dt_{coarse}}$ which is given by

$$\frac{dV_{out}}{dt_{coarse}} = \frac{I_{coarse}}{C_{CLS} + \frac{C_{FB}C_{IN}}{C_{FB} + C_{IN}}} = \frac{I_{coarse} + \frac{V_{out}}{r_{o,coarse}}}{C_{CLS} + \frac{C_{FB}C_{IN}}{C_{FB} + C_{IN}}} =$$

$$= \frac{(I_{coarse} + \frac{V_{out}}{r_{o,coarse}})(C_{FB} + C_{IN})}{C_{FB}C_{CLS} + C_{IN}C_{CLS} + C_{FB}C_{IN}} \quad (3)$$

where $r_{o,coarse}$ is the output impedance of current source I_{coarse}. Substituting Eq. (2) into Eq. (1) gives

$$I_{fine} = I_{fine0} - \left(\frac{C_{FB}C_{CLS} + C_{IN}C_{CLS} + C_{FB}C_{IN}}{C_{FB}C_{CLS} + C_{IN}C_{CLS}}\right) \times \left[\frac{\left(I_{coarse} + \frac{V_{out}}{r_{o,coarse}}\right)\left(C_{FB} + C_{IN}t_{delay,coarse}\right)}{(C_{FB}C_{CLS} + C_{IN}C_{CLS} + C_{FB}C_{IN})r_o}\right] \quad (4)$$

$$= I_{fine0} - I_{coarse0}\left(\frac{t_{delay,coarse}}{r_o C_{CLS}}\right) - \left(\frac{V_{out}}{r_o}\right)\left(\frac{t_{delay,coarse}}{r_{o,coarse}C_{CLS}}\right),$$

Assuming that $t_{delay,coarse}$ is a constant, the $I_{coarse0}$ term is a constant. The $\frac{V_{out}}{r_o}$ term represents the new output dependence of I_{fine} on V_{out}. We see from Eq. (3) that the output resistance of I_{fine}, has effectively been multiplied:

$$r_{o,CLS} = \left(\frac{r_{o,coarse}C_{CLS}}{t_{delay,coarse}}\right) \quad (5)$$

To further improve output impedance of the gated current source I_{fine} , one can use also cascoding technique but this would require more voltage headroom and thus more voltage on power supple rails. As year by year, due to the scaling of CMOS technologies, the power supply voltage is reduced, the latter case of using cascoding structure to have more output resistance of current source has not investigated.

Note that for large values of C_{CLS}, I_{fine} is able to pull V_{out} beyond V_{DD}. So this will reduce life-tie and reliability of transistors. So in the design stage it is needed verify that the voltage will not exceed beyond the power supply rails.

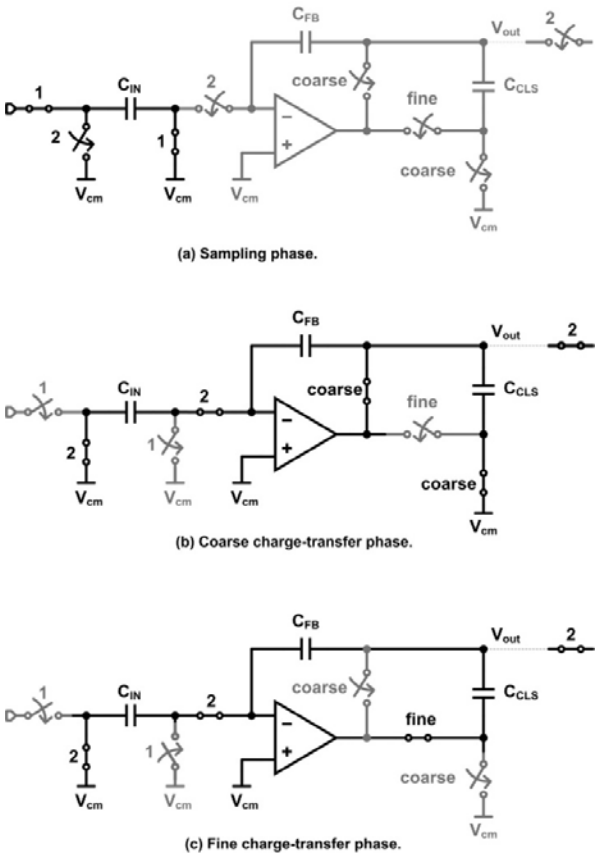

Fig. 1. Correlated level shifting technique. Sampling phase, $\boldsymbol{\varphi_1}$ = "1"; charge-transfer phase (preset + coarse), $\boldsymbol{\varphi_2}$ = "2".

IV. SIMULATION RESULTS

The transfer functions of the conventional integrator of Fig. 1 (but without CLS capacitor), and the proposed CLS integrator of Fig. 2 was simulated with HSPICE using SNAC (Shooting Newton AC) analysis. The DC gain of the opamp was chosen to be 27 dB and the capacitors were chosen such that $C_{FB} = C_{LS} = C_{CLS}$, where C_S is 150fF. As can be seen from Fig. 3, the conventional integrator has a low frequency gain of 27 dB, while CLS integrator obtain a low-frequency gain of 54 dB (double that of the conventional). The integrator was also used to design 2-0 MASH (the multi-stage noise shaping) modulators. The op-amp DC gain was maintained at 27 dB while the two integrators in the loop were designed to have a closed-loop gain of 0.5 V/V each.

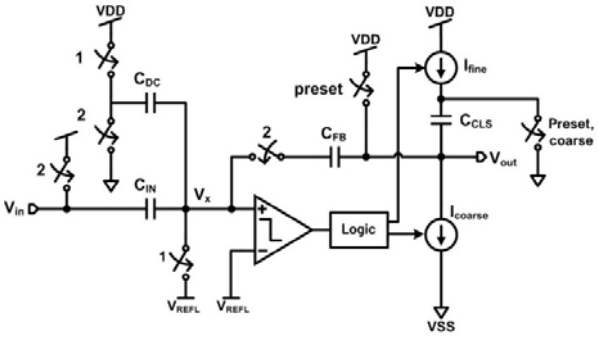

Fig. 2. Correlated level-shifting used in switched capacitor integrator: Sampling phase, $\boldsymbol{\varphi_1}$ = "1"; charge-transfer phase (preset + coarse + fine), $\boldsymbol{\varphi_2}$ = "2".

Simulation results from MATLAB in Fig. 4 show that the modulator with the conventional integrator suffers the worst quantization noise leakage. It achieves an SQNR of 65.0 dB at an OSR of 64 while the modulators with CLS integrator achieve an SQNR 86.0 dB. The difference in SQNR between the conventional and the proposed technique is because the effective low-frequency gain is 54 dB in the proposed integrator and a twice lower gain in the conventional integrator.

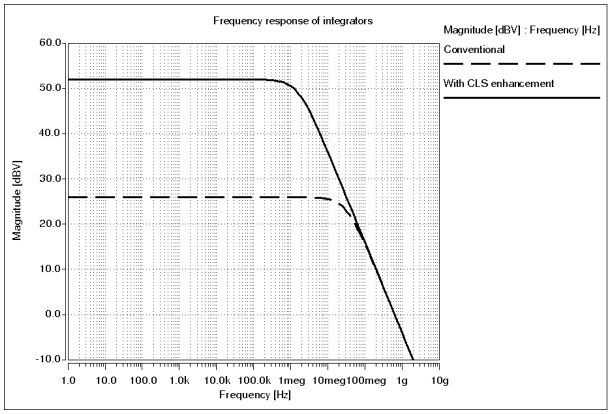

Fig. 3. Simulated frequency response of integrators

V. CONCLUSION

A gain enhancement technique has been proposed for comparator-based integrators. Theoretical analysis of the loop gain enhancement has been proved for comparator based integrator with correlated level shifting technique applied, which is successfully observed and approved with HSPICE/MATLAB simulations. Also proposed comparator based integrator with correlated level shifting enhancement was used to build 2-0 MASH sigma-delta modulator which achieves a SQNR of 86.0 dB at an OSR of 64.

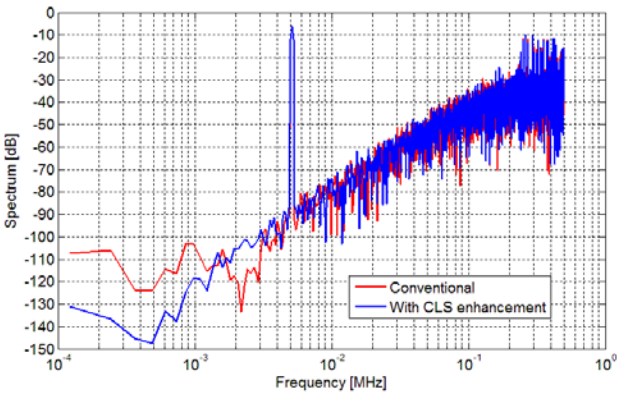

Fig. 4. Simulated output spectra of modulators

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